Cisco Silicon One Q202 and Q202L Processors

Contents

The silicon industry has always been plagued with the trichotomy of switching silicon, routing line card silicon, and routing fabric silicon. Using these three basic building blocks, silicon and system vendors created unique architectures tuned for individual markets and industries. Consequentially, forcing customers to consume and manage these disjointed and dissimilar products caused an explosion in complexity, CapEx, and OpEx for the industry.

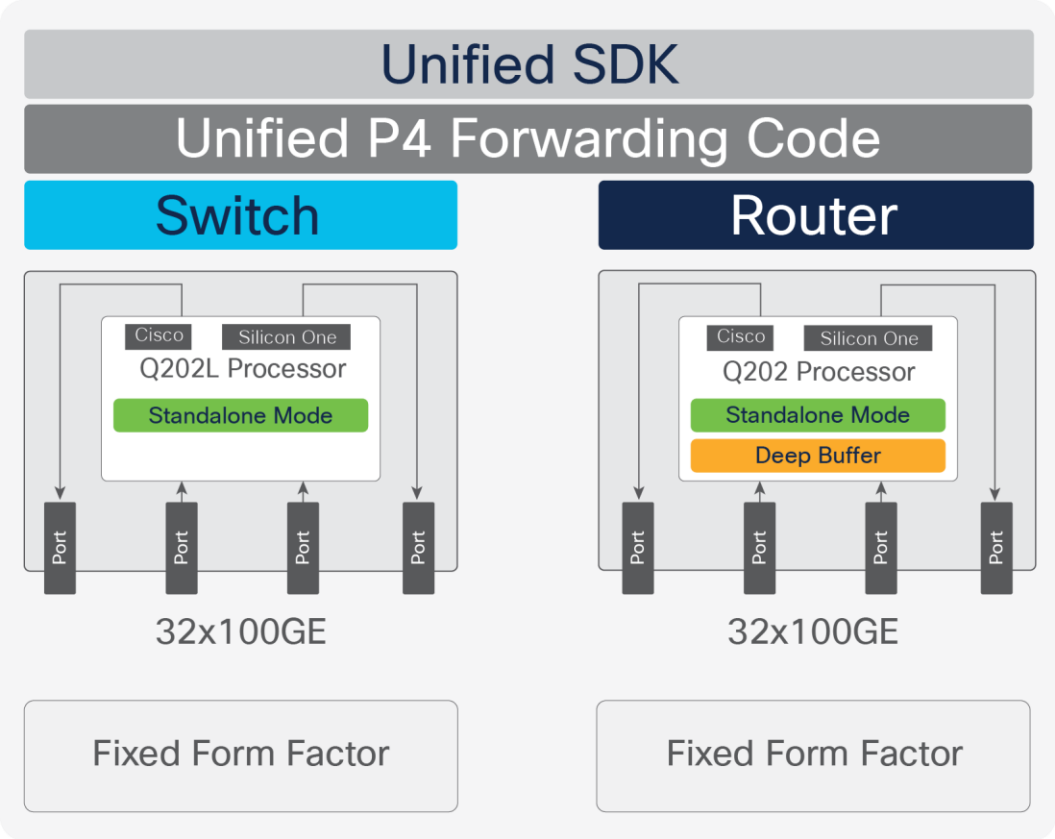
The Cisco Silicon One™ architecture ushers in a new era of networking, enabling one silicon architecture to address a broad market space, while simultaneously providing best-of-breed devices.

At 3.2 Tbps, the Cisco Silicon One Q202L builds on the ground-breaking technology of the Cisco Silicon One Q200L but brings the efficiency and flexibility of Cisco Silicon One and 7 nm down to the 32x100GE Top-of-Rack (ToR) switches. The Q202 provides similar advantages for the WAN and peering routers, enabling a 32x100GE deep-buffered and high-scale router.

Product overview

The Cisco Silicon One Q202 processor is a 3.2-Tbps, full-duplex, standalone routing processor with deep buffers, while the Cisco Silicon One Q202L is a 3.2-Tbps, full-duplex, standalone switching processor.

Cisco Silicon One Q202 can be used to build fixed form factor routers ideally targeted for peering, lean edge, and access applications. The Cisco Silicon One Q202L can be used to build fixed form factor switches ideally targeted for data center Top-of-Rack (ToR) applications.



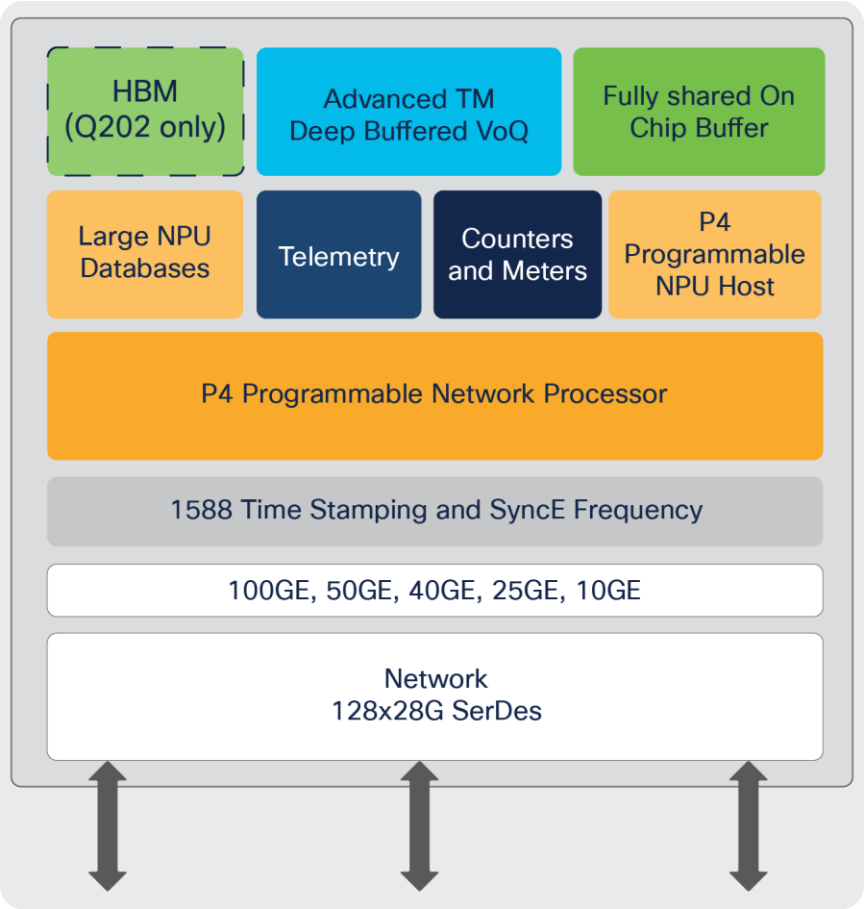
Features and benefits

Table 1. Architectural Characteristics and Benefits

Feature	Benefit
Unified architecture across multiple markets	Greatly simplifies customer network infrastructure deployments
Unified SDK across market segments and applications	Provides a consistent point of integration for all applications across the entire network infrastructure
High-performance routing and switching silicon	Achieve line rate at small packet sizes
Power-efficient routing and switching silicon	The power efficiency of 7 nm and the Cisco Silicon One architecture
Large and fully unified packet buffer	Fully shared on-die buffer with optional large, external packet buffer
Switching efficiency with routing features and scale	Addresses the requirements of service provider and web-scale providers' routing and switching applications
Run-to-completion network processor	Provides feature flexibility without compromising performance or power efficiency
P4 programmable	Leverages an open-source programming language to enable customers to define their own features

Prominent feature

Flexibility, Performance, and Scale for Next-Generation Service Provider and Web-Scale Networks



Features

- 128 28G SerDes; each can be configured independently to operate in 10G/25G using NRZ modulation
- Flexible port configuration supporting 10/25/40/50/100 Gbps
- Large, fully shared, on-die packet buffer
- Large, in-package packet buffer (Q202 only)
- 1588v2 and SyncE support with nanosecond-level accuracy
- On-chip, high-performance, P4-programmable host NPU for high-bandwidth offline packet processing (for example, OAM processing, MAC learning)
- Multiple embedded processors for CPU offloading

Traffic Management

- Large pool of configurable queues, supporting DiffServ and hierarchical QoS
- Support for system-level, end-to-end QoS and scheduling for both unicast and multicast traffic
- Seamless extension of on-die buffer to external packet buffer
- Support for ingress and egress traffic mirroring
- Support for link-level (IEEE802.3x), PFC priority-level (802.1Qbb) flow control and ECN Marking
- Support of port extenders

Network Processor

- Run-to-completion, P4-programmable network processor
- Line rate at very small packets even with complex packet processing
- Large and shared fungible tables
- Support for complex packet processing features without impacting data rate
- Support for simple packet processing features with optimized power and latency

Load Balancing

- Flow load balancing using ECMP or LAG
- Dynamic flowlet load balancing with ability to detect and handle elephant flows

Instrumentation and Telemetry

- Programmable meters used for traffic policing and coloring
- Programmable counters used for flow statistics and OAM loss measurements
- Programmable counters used for port utilization, microburst detection, delay measurements, flow tracking, elephant flow detection, and congestion tracking
- Traffic mirroring: (ER)SPAN on drop
- Support for sFlow and NetFlow

SDK

- APIs provided in both C++ and Python
- Configurability via high-level networking objects
- Distribution-independent Linux packaging
- Robust simulation environment enables rapid feature development
- CPU packet I/O through native Linux network interfaces

P4 Programmability

- Application development is handled by a P4-based IDE programming environment
- At compilation, the P4 application generates low-level register/memory access APIs and higher-level SDK Application APIs
- Provides application support for a wide range of data center, service provider, and enterprise protocols
- Modifications to the provided application can be easily accomplished using the provided P4 development environment
- Ability to develop the SDK and applications running over the SDK over a simulated Cisco Silicon One device

Cisco P4 Application

Due to Silicon One's extensible P4 programming toolkit, we are always adding features to address new markets and new customer requirements; however, a sample of the features that are currently available with the P4 code is provided below:

- IPv4/v6 Routing
  - OSPF
  - IS-IS
  - BGP
- MPLS Forwarding
  - LDP, LDPoTE
  - RSVP-TE
  - SR-MPLS
  - SR-TE
  - L3VPN, 6PE, 6VPE
  - BGP LU
  - VPWS/EoMPLS
  - VPLS
- Ethernet Switching
  - 802.1d, 802.1p, 802.1q, 802.1ad
- IP Tunneling
  - IPinIP
  - GRE
  - VXLAN
- Integrated Routing and Bridging (IRB)
- HSRP/VRRP
- Policy-Based Routing
- Security and QoS ACLs
- ECMP and LAG (802.3ad)
- Multicast
  - PIM-SM/SSM
  - IGMP
  - MLDP
  - MVPN
- NAT/PAT
- Protection (Link/Node/Path and TI-LFA)
- QoS Classification and Marking
- Congestion Management
- Telemetry
  - NetFlow, sFlow
  - (ER)SPAN
  - Packet Mirroring with Appended Metadata
  - Lawful Intercept
- DDoS Mitigation
  - Control-Plane Policing
  - BGP Flowspec
- Timing and Frequency Synchronization
  - SyncE
  - 1588

Product sustainability

Information about Cisco's Environmental, Social, and Governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability reporting.

Table 2. Cisco Environmental Sustainability Information

Sustainability Topic		Reference
General	Information on product-material-content laws and regulations	Materials
	Information on electronic waste laws and regulations, including our products, batteries, and packaging	WEEE Compliance
	Information on product takeback and resuse program	Cisco Takeback and Reuse Program
	Sustainability inquiries	Contact: csr_inquiries@cisco.com
Material	Product packaging weight and materials	Contact: environment@cisco.com

For more information

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Cisco Systems (USA) Pte. Ltd.
Singapore

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The Netherlands

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